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Title of the Invention

Semiconductor Device and Manufacturing Method Thereof

Background of the Invention

The present invention relates to a semiconductor device, and more specifically, it relates to a resin-sealed semiconductor device and a manufacturing method thereof.

With mobile apparatuses such as notebook computers having come to be used widely in recent years, resin-sealed semiconductor devices mounted in such apparatuses need to achieve a lower profile, further miniaturization and reduced weight. Accordingly, numerous resin-sealed semiconductor devices have been proposed in response to these technical requirements.

FIG. 4 illustrates an example of such a semiconductor device in the prior art. Wiring 104 constituted of copper (Cu) are electrically connected to electrode pads 102 formed at the primary surface of a semiconductor element 100. Cu posts 106 having a height of approximately 150 micrometer are connected with the wiring 104. Then, a resin layer 108 is formed at a height corresponding to the height of the Cu posts 106 for sealing. External connection terminals constituted of a metal such as solder balls 110 are formed at the tips of the Cu posts 106 that are exposed.

The process up to this point is implemented on a wafer with a plurality of semiconductor elements 100 arrayed thereon. Then, the wafer undergoes a dicing process to be divided into individual pieces. The resulting semiconductor devices are so-called chip-size package semiconductor devices whose size is very close to the size of the semiconductor elements.

During the process for manufacturing the device described above, a wafer comprising a plurality of semiconductor elements 100 is

set at a mold die constituted of an upper die 112 and a lower die 114, as illustrated in FIG. 5, to achieve sealing with a resin so as to completely cover the Cu posts 106.

If foreign matter such as dirt is present inside the mold die at this time, the foreign matter may come into contact with the rear surfaces of the semiconductor elements 100 to scar them and even cause cracks 116.

In addition, surface polishing is performed by using an abrasive material 118, as illustrated in FIG. 6 to expose the tips of the Cu posts 106 after the resin curing process.

During the polishing process, the wafer is vacuum held through vacuum holes 122 formed at a polishing stage 120 to secure the wafer. However, if the wafer is warped, the vacuum hold may not be successful, which, in turn, may make it impossible to perform surface polishing.

Such warping of the wafer occurs due to the difference between the coefficient of expansion of the wafer (the semiconductor element 100) and the coefficient of expansion of the resin layer 108 sealed thereupon. Such warping occurs to varying degrees depending upon the thickness of the resin layer 5 and the type of material used to constitute the resin layer 5.

In addition, semiconductor devices achieved by forming a sealing resin layer at the rear surfaces of the semiconductor elements as well as at the primary surfaces have been proposed in recent years. However, there is a problem in that since the resin is injected at both surfaces, the total thickness of the resin layer increases.

Summary of the Invention

By addressing the problems of the prior art discussed above, according to the present invention, the primary surface of a

semiconductor element is sealed with a resin layer and protective tape is bonded to its rear surface.

Brief Description of the Drawings

The above and other features of the invention and the concomitant advantages will be better understood and appreciated by persons skilled in the field to which the invention pertains in view of the following description given in conjunction with the accompanying drawings which illustrate preferred embodiments.

FIG. 1 is a sectional view of an embodiment of the present invention;

FIG. 2 illustrates the manufacturing method according to the present invention (part 1);

FIG. 3 illustrates the manufacturing method according to the present invention (part 2);

FIG. 4 is a sectional view of a structure adopted in the prior art;

FIG. 5 illustrates a resin sealing process implemented in the prior art; and

FIG. 6 illustrates a surface polishing process implemented in the prior art.

Detailed Description of the Preferred Embodiment

The following is a detailed explanation of the semiconductor device and the manufacturing method thereof in a preferred embodiment of the present invention given in reference to the attached drawings.

FIG. 1 is a sectional view of the semiconductor device in an embodiment of the present invention. The method that is employed to manufacture this semiconductor device is explained. First, electrode pads 12 are formed at the primary surface of semiconductor elements

10. Next, wirings 14 constituted of Cu which are to function as means for electrical connection are connected to the electrode pads 12. Then Cu posts 16 constituting means for electrical connection are connected to the wirings 14 and are formed to achieve a specific height. The primary surfaces of the Cu posts 16 are then sealed with a resin layer 18. Then, solder balls 20 constituting external connection terminals are mounted at the exposed tips of the Cu posts 16.

In this embodiment, protective tape 22 is bonded to the rear surfaces of the semiconductor elements 10. The protective tape 22, which is constituted of a hardened synthetic resin achieving a bonding function such as polyimide or an epoxy resin, protects the rear surfaces of the semiconductor elements 10, which are constituted of a fragile material.

As explained above, since the rear surfaces of the semiconductor elements 10 are protected by bonding the protective tape 22 in the embodiment of the present invention, cracking due to any external force that may be applied to them or due to contact with foreign matter is prevented from occurring. In addition, since only the primary surfaces of the semiconductor elements 10 are sealed with the resin and their rear surfaces are bonded with the protective tape 22, resin injection must be implemented only at one side to facilitate the filling process, and a chip-size package semiconductor device achieving a low profile is realized.

FIG. 2 shows the semiconductor device manufacturing method according to the present invention by presenting individual manufacturing steps in sectional views.

FIG. 2(a) illustrates a step in which a wafer having a plurality of semiconductor elements 10 formed thereon is prepared. As has already been explained, the electrode pads 12 are formed at the primary surfaces of the individual semiconductor elements 10, with

the wirings 14 constituted of Cu and the Cu posts 16 both to function as a means for electrical connection connected to the electrode pads 12

FIG. 2(b) illustrates a step in which the protective tape 22 in a size roughly the same as the size of the wafer is bonded to the rear surface of the wafer. It is to be noted that the illustration of the electrode pads 12 and the wirings 14 is omitted in FIG. 2(b) and the subsequent drawings.

The protective tape 22 may be applied through bonding onto the rear surface of the wafer by adopting a method similar to that employed for the application of regular dicing tape.

FIG. 2(c) illustrates the resin sealing step. The wafer with the protective tape 22 applied onto the rear surface thereof is set at a mold die constituted of an upper die 24 and a lower die 26. Then, a resin is injected to completely cover the Cu posts 16. Next, a heat treatment is performed to form the resin layer 18 so that the primary surfaces of the semiconductor elements 10 become sealed with resin.

At this point, since the rear surface of the wafer (the semiconductor elements 10) is covered by the protective tape 22, foreign matter such as dust inside the die does not come into contact with the rear surface of the wafer and also, the strength is improved. As a result, it is possible to prevent cracks from occurring at the semiconductor elements 10. Moreover, the wafer does not become warped as readily as in the prior art.

FIG. 3(d) illustrates a surface polishing process in which the wafer is secured to a polishing stage 28 through vacuum holding achieved through the vacuum holes 30.

Since the protective tape 22 is bonded to the rear surface of the wafer in the embodiment, the warping of the wafer can be minimized, unlike in the prior art and, as a result, the wafer is secured squarely

onto the polishing stage 28. Thus, the resin layer can be polished accurately with a high degree of reliability by using an abrasive material 32 until the tips of the Cu posts 16 become exposed.

The wafer would be caused to become warped due to the difference between the coefficient of expansion of the wafer (the semiconductor elements 10) and the coefficient of expansion of the resin layer 18 sealing the primary surface of the wafer. However, by applying the protective tape 22 to the rear surface, a good balance is achieved with respect to expansion and contraction occurring at the front and rear of the wafer in the embodiment to reduce the degree of warping. Thus, the wafer can be secured onto the polishing stage 28 with greater ease to enable surface polishing to be performed accurately with a high degree of reliability.

FIG. 3(e) illustrates a step in which the solder balls 20 constituting external connection terminals are mounted at the tips of the Cu posts 16 exposed at the surface of the resin layer 18.

FIG. 3(f) illustrates a step in which the wafer having undergone the steps described above is cut along cutting lines 36 by a cutting blade 34 to be divided into individual pieces.

While the semiconductor device in the embodiment achieves a lower profile, since only one surface of the semiconductor element 10 is sealed with resin as explained earlier, the rear surface of the wafer is polished to achieve an even lower profile.

During this rear surface polishing, which is implemented following the surface polishing step illustrated in FIG. 3(d), the protective tape 22 is first peeled from the rear surface of the wafer through UV (ultraviolet ray) irradiation and then the rear surface is polished. Since no heat treatment is performed at this point, no problem occurs if the protective tape 22 is peeled off.

It is to be noted that while the wirings 3 and the Cu posts 16 constitute means for electrical connection and the solder balls 20 constitute external connection terminals in the example explained above, the present invention is not restricted to this example.

While the semiconductor device and the manufacturing method thereof have been particularly shown and described with respect to a preferred embodiment thereof by referring to the attached drawings, the present invention is not limited to this example and it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit, scope and teaching of the invention.

As explained above, according to the present invention, in which the protective tape is bonded onto the rear surface of a semiconductor element, occurrence of cracks due to an external force or the presence of foreign matter can be prevented, and since only the primary surface of the semiconductor element is sealed with resin, the process of injecting the resin is facilitated and a lower profile is achieved.

Furthermore, since the protective tape is bonded onto the rear surface of the wafer before the resin sealing step, scarring of the wafer can be reduced and warping of the wafer can be prevented during the resin sealing step, to facilitate the surface polishing step.

The entire disclosure of Japanese Patent Application No. 11-29479 filed on February 8, 1999 including specification, claims, drawings and summary is incorporated herein by reference in its entirety.